IN THE CLAIMS

Below, please find a clean, unmarked copy of the claims. Claims 1-19 are re-presented. Please add new claims 26-32.

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1. A method of forming a transistor, comprising:

forming an alignment component on a substrate of a semiconductor material, said alignment component consisting of a single material;

depositing a metal layer over the substrate and the alignment component;

reacting the metal layer with the semiconductor material of the substrate to form two silicide regions, the silicide regions having inner surfaces which face one another, wherein an upper portion of each inner surface contacts the alignment component and a lower portion of each inner surface contacts the semiconductor material of the substrate;

removing the alignment component; and

replacing the removed alignment component with a conductive gate.

2. The method of claim 1 wherein the alignment component is non-conductive.

3. The method of claim 2 wherein the alignment component is made of a material selected from the group consisting of a silicon oxide and silicon nitride.

4. The method of claim 1 wherein the alignment component is made of a material which does not react with the metal layer when the metal layer is reacted with the semiconductor material of the substrate.

5. The method of claim 1 wherein the alignment component has a thickness of between 1000Å and 2500Å.

6. The method of claim 1 wherein the alignment component is less than 0.10 microns wide.

7. The method of claim 1 wherein the metal layer is selected from the group consisting of a material comprising tungsten, cobalt and titanium.

8. The method of claim 1 wherein the metal layer is between 300Å and 400 Å thick.

9. The method of claim 1 wherein the silicide regions have lower surfaces located lower than a lower surface of the alignment component.

10. The method of claim 1 wherein removing the alignment component comprises:

depositing a layer over the silicide regions and the alignment component;

planarizing the layer at least until the alignment component is exposed; and

etching the alignment component at least until the substrate is exposed to leave an opening between the inner surfaces of the silicide regions to allow for formation of the gate.

11. The method of claim 10 wherein, after the etching of the alignment component, the upper portions of the inner surfaces are exposed.

12. The method of claim 10 wherein the alignment component and the layer are made of different materials, one being made of a silicon oxide and the other being made of silicon nitride.

13. The method of claim 1 wherein the gate is formed according to a method comprising:
depositing a gate dielectric layer; and
forming a gate electrode on the gate dielectric layer.

14. The method of claim 13 wherein the gate dielectric layer is less than 10Å thick.

15. The method of claim 13 wherein the gate electrode is made out of a metal.

16. The method of claim 1, further comprising:
forming doped regions which extend from the silicide regions in underneath the gate.

17. The method of claim 13 wherein the gate dielectric layer has a dielectric constant of at least 100.

18. The method of claim 13 wherein the gate dielectric layer comprises a material selected from the group consisting of strontium titanate, and barium strontium titanate.

19. The method of claim 17 wherein the gate electrode comprises a material selected from the group consisting of platinum, a conductive metal oxide, and ruthenium oxide.

26. (New) A method of forming a transistor, comprising:

forming an alignment component on a substrate of a semiconductor material;

forming two silicide regions aligned with the alignment component, the silicide regions having inner surfaces which face one another, wherein an upper portion of each inner surface contacts the alignment component and a lower portion of each inner surface contacts the semiconductor material of the substrate forming a Schottky junction;

removing the alignment component to expose the substrate and the upper portions of each inner surface of the silicide regions;

depositing a gate dielectric layer on the substrate and the upper portions of each inner surface of the silicide regions; and

forming a gate electrode on the gate dielectric layer.

27. (New) The method of claim 26, wherein forming the two silicide regions comprises:

depositing a metal layer over the substrate and the alignment component; and

reacting the metal layer with the semiconductor material of the substrate.

28. (New) The method of claim 27, wherein the metal layer is made of cobalt or nickel and the silicide regions extend partially below the alignment component.

29. (New) The method of claim 27, wherein the alignment component is made of a material that does not react with the metal layer when the metal layer is reacted with the semiconductor material of the substrate.

30. (New) The method of claim 29, comprising removing a portion of the metal layer above the alignment component after the metal layer is reacted with the semiconductor material of the substrate.

31. (New) The method of claim 26, wherein the gate dielectric layer is made of silicon oxide and has a thickness of less than 10 Å.

32. (New) The method of claim 26, wherein removing the alignment component comprises:

depositing a layer of a different material than the alignment component over the silicide regions and the alignment component;

planarizing the layer at least until the alignment component is exposed; and

etching the alignment component at least until the substrate and the upper portions of each inner surface of the silicide regions are exposed.